Ario Kianazad

Website: ariokian.com
Email: a.kianazad@mail.sbu.ac.ir
LinkedIn: linkedin.com/in/ario-kian/
Scholar: Ario Kian

About Me

FPGA based Embedded System Researcher and Side-Channel Analyzer. Graduated from Shahid Beheshti University, Faculty of Computer Science and Engineering in Master's Degree, member of the Integrated Circuits Automated Design Lab, with research background in designing secure dynamically reconfigurable systems against Side-Channel Analysis Attacks with 1 published paper in CADs 2020 Conference.

Education

Shahid Beheshti University, Tehran, Iran — GPA(Total): 3.4/4
M.S. in Computer Engineering (Computer Systems Architecture) — Sep 2016–Sep 2019

- Research Area: "Hardware Security Analysis of Reconfigurable Systems"
- Thesis: "Security Improvement of FPGA-based Design Against Side-Channel Analysis Attacks using Dynamic Partial Reconfiguration"

Guilan University, Guilan, Iran — GPA(Last two years): 3.1/4
B.S. in Computer Engineering (Hardware Engineering) — Sep 2011–Dec 2015

Publications

[1] A. Kian, H. Hosseintalaee, and A. Jahanian, "Protecting the FPGA IPs against higher-order side channel attacks using dynamic partial reconfiguration", in *2020 20th International Symposium on Computer Architecture and Digital Systems (CADS)*, Aug. 2020, pp. 1–4.

- Link: https://ieeexplore.ieee.org/abstract/document/9211862

In Preparation:
- Title: Analytical Review on the Side-Channel Security Aspect of Partial Reconfigurable Systems
- Authors: Ali Jahanian; Milad Salimian; Ario Kian

Skills

- **HDL Languages:** VHDL, Verilog
- **Programming Languages:** C/C++, Matlab, Python, Javascript, Angular, NodeJS, SQL
- **Tools and IDEs:** Vivado Design Suite, ISE Design Suite, Matlab, Simulink, Altium Designer, Eclipse IDE, Keil uVision5, Visual Studio Code
- **Platforms:** Xilinx FPGAs, Zynq APSoC, Raspberry Pi, Arduino, STM32 Microcontrollers

Honors and Awards

- 5th National Digital System Design Contest of Iran — Dec 5th-6th 2018
  Branch : ASIC Design
  Contest Topic: Design and implementation of a Direct Digital Synthesizer (DDS)
  Ranking: Third Place

Teaching Experience

- **Teaching Assistant** at Shahid Beheshti University   Spring 2019
  Embedded System Design Modeling and Methodology (MSc Degree Course)
  Lecturer: Dr.Seyed-Hosein Attarzadeh-Niaki

- **Teaching Assistant** at Shahid Beheshti University   Spring 2018
  Computer Architecture Lab (BSc Degree Course)
  Lecturer: Dr.Zohre Beiki

- **Teaching Assistant** at Shahid Beheshti University   Fall 2017
  Computer Architecture Lab (BSc Degree Course)
  Lecturer: Dr.Zohre Beiki

- **Head Teaching Assistant** at Shahid Beheshti University   Spring 2017
  Digital Circuit, Logic and Design (BSc Degree Course)
  Lecturer: Dr.Ali Jahanian

- **Head Teaching Assistant** at Shahid Beheshti University   Fall 2016
  Digital Circuit, Logic and Design (BSc Degree Course)
  Lecturer: Dr.Ali Jahanian

Work Experience

SEA (Speed Energy Aryanic)   Tehran, Iran
Embedded Developer/Altium PCB Designer (Part-time)   Oct 2020 - Present

Mana Pardaz Control   Tehran, Iran
FPGA Interface Developer (Full-time)   Mar 2020 - Sep 2020

Nano Afzar Tarashe   Tehran, Iran
Embedded System Developer and Researcher (Part-time)   May 2017 - Mar 2020

Course Projects

- Differential Power Analysis(DPA) attack on AES Cryptography Standard
  (Hardware Security MSc Course)

- HDL based implementation of a dynamic size Butterfly structure for a Netwrok-on-Chip processing System
  (Parallel Processing MSc Course)

- HDL based implementation of floating-point divider unit
  (Computer Arithmetic MSc Course)

- Implementation of Simulated-Annealing algorithm for resource placement optimization in ASIC placement and routing tools
  (VLSI Design Automation Algorithms MSc Course)

- Implementation of Real-Time Arduino based Elevator Control Unit using freeRTOS
  (Embedded System Design Modeling and Methodology)

Work Projects

- Implementation of UART Serial Interface in HDL for Xilinx Artix-7 FPGA
  (Mana Pardaz Control)

- Extraction of Xilinx FPGAs DNA Code and Use it for preventing the cloned design to be executed on other Devices
  (Mana Pardaz Control)

- Area based Optimization of HDL Projects using Specific Embedded Resources in Xilinx FPGAs such as BRAMs, DSP blocks
  (Mana Pardaz Control)
- Sampling of data passing through Data and Control Bus from a custom processing platform using ChipScope environment
  (Mana Pardaz Control)
- Sampling of data passing through Data and Control Bus from a custom processing platform using ChipScope environment
  (Mana Pardaz Control)
- Development of a minimal Embedded Web Server using NodeJS
  (Speed Energy Aryanic)
- PCB Design for Battery State Monitoring Devices
  (Speed Energy Aryanic)
- Development of a Control Unit for a Step Based Stabilizer
  (Speed Energy Aryanic)
- Development of a Control Unit for an Automatic Transfer Switch(ATS)
  (Speed Energy Aryanic)
- Research on SNMP based Monitoring and Controling Devices Specific for Uninterruptible Power Supplies(UPS)
  (Nano Afzar Tarashe)
- Test and Analysis of the Claimed Specifications and Parameters of UPS devices from Different Vendors
  (Nano Afzar Tarashe)

REFERENCES

- Ali Jahanian: Assistant Professor, Faculty of Computer Science and Engineering, Shahid Beheshti University
  Email: jahanian@sbu.ac.ir
  Home Page: http://facultymembers.sbu.ac.ir/jahanian/
  Scholar Page: Ali Jahanian (https://scholar.google.com/citations?user=gTht4nwAAAAJ&hl=en)
- Zohre Beiki: Assistant Professor, Faculty of Computer Engineering, University of Isfahan
  Email: z.beiki@eng.ui.ac.ir
  Home Page: https://engold.ui.ac.ir/ z.beiki/
  Scholar Page: Zohre Beiki (https://scholar.google.com/citations?user=kYgnTKoAAAAJ&hl=en)